TOSHIBA

Leading Innovation

Panel Discussion: EUVL HVM Insertion and Scaling

Readiness and Challenges of EUV Mask

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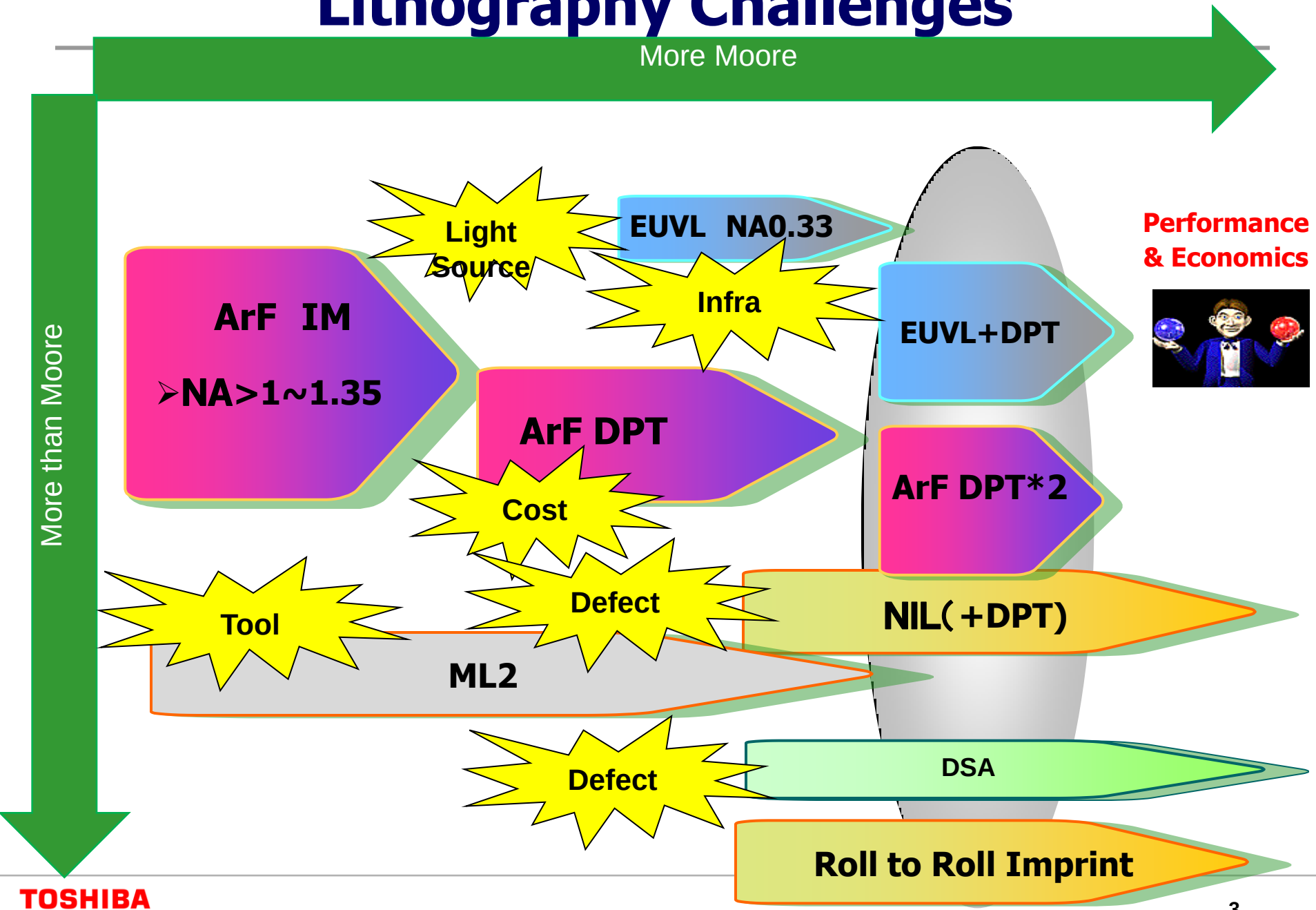
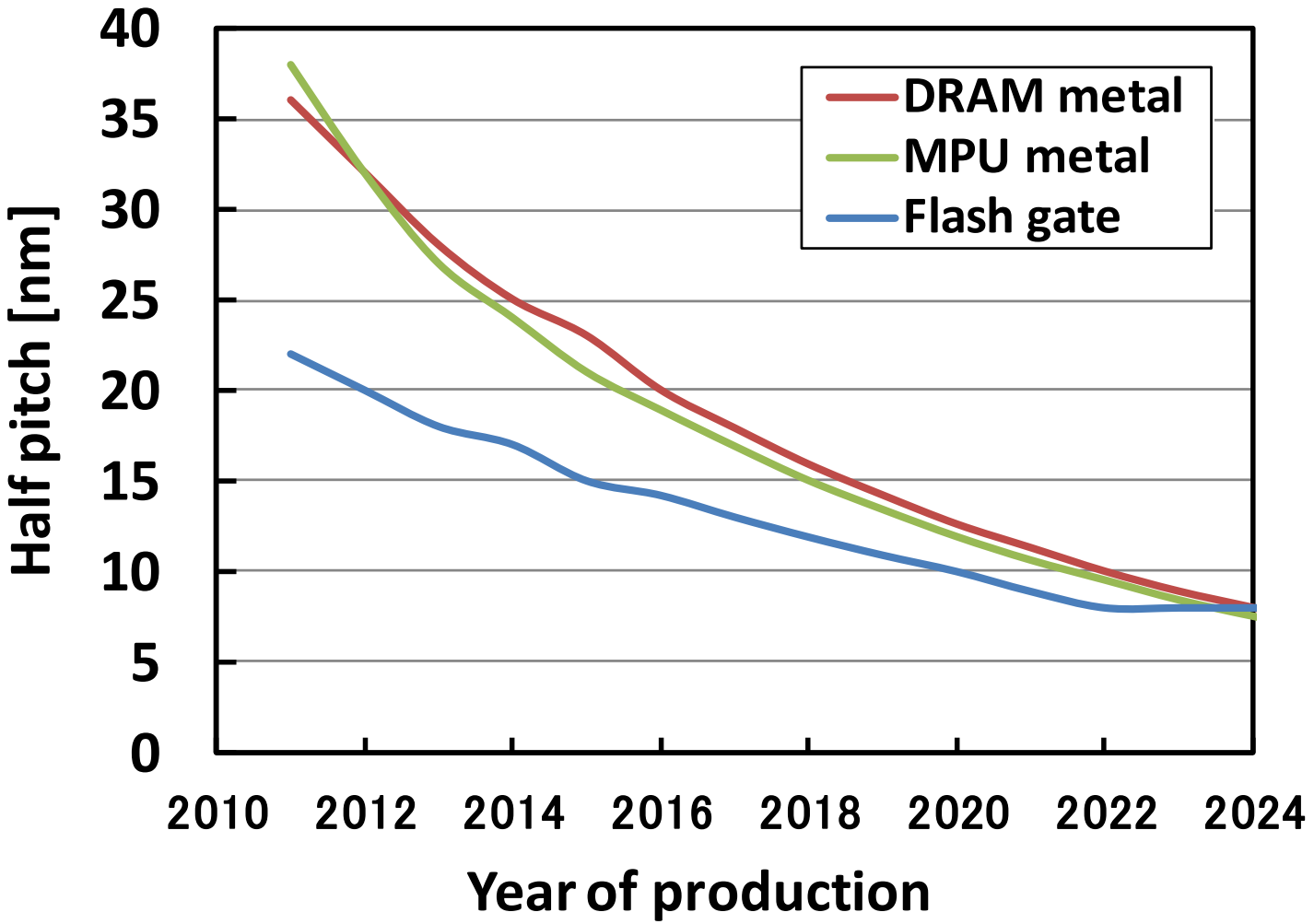
Contents

Lithography Challenges

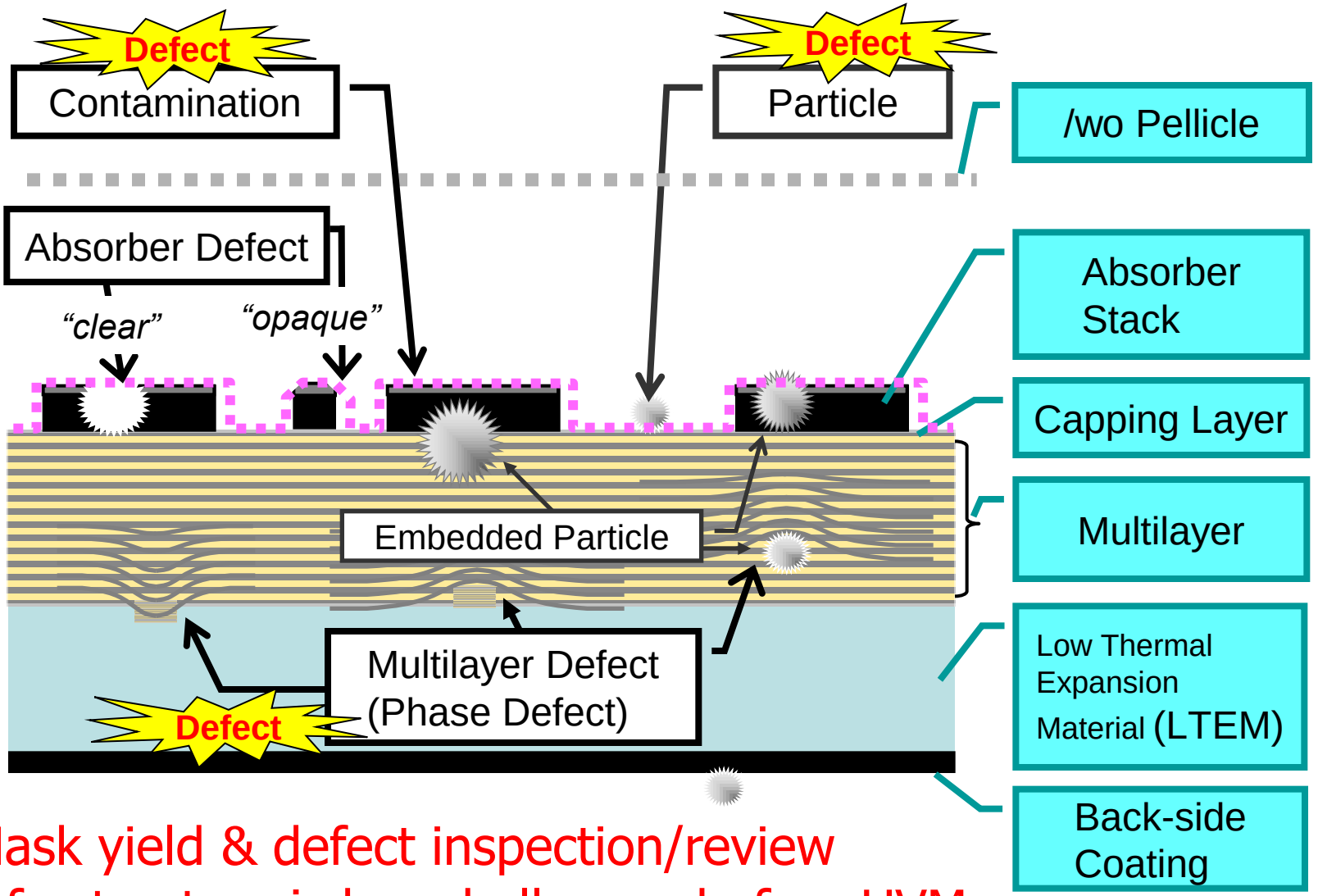


Scaling Road Map



Ref: ITRS 2011 Edition Table B *"Key Lithography-related Characteristics by Product"*

Current EUV Mask Structure and Challenges

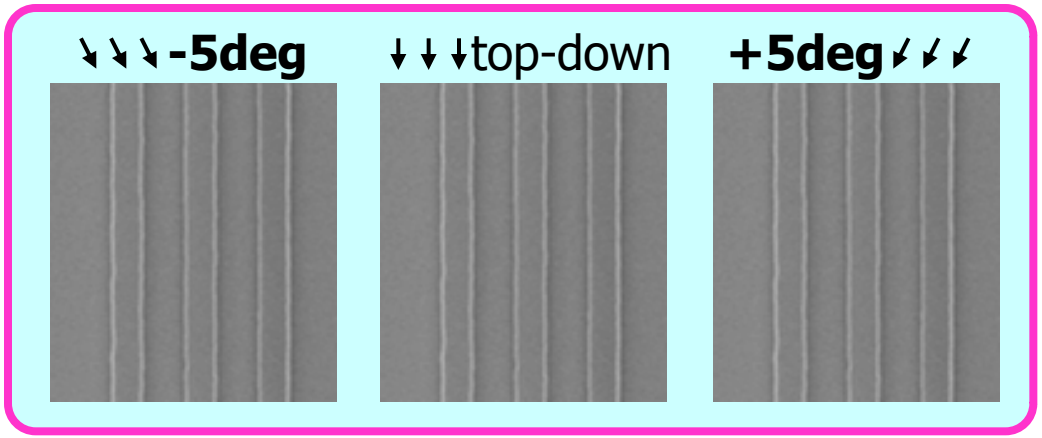


Mask yield & defect inspection/review infrastructure is key challenges before HVM.

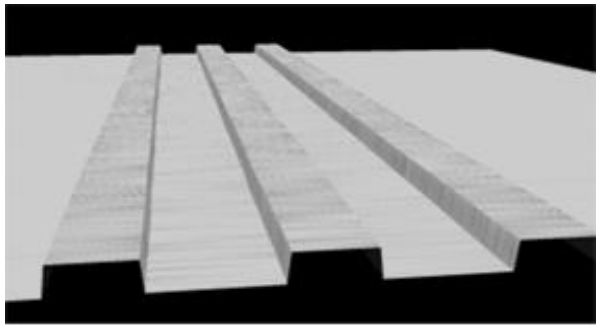
QA of Repaired Absorber Pattern

- EUV-AIMS will not available at the early stage of HVM.
- 3D SEM + Litho. simulation is applied to bridge the gap.

Top-down & tilted SEM images of mask pattern

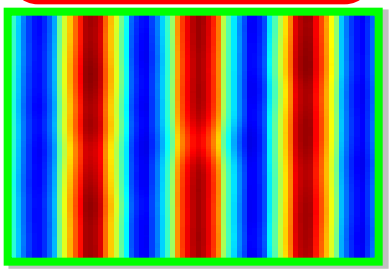


UR-7T (TOPCON)



3D mask image

Prediction of wafer image

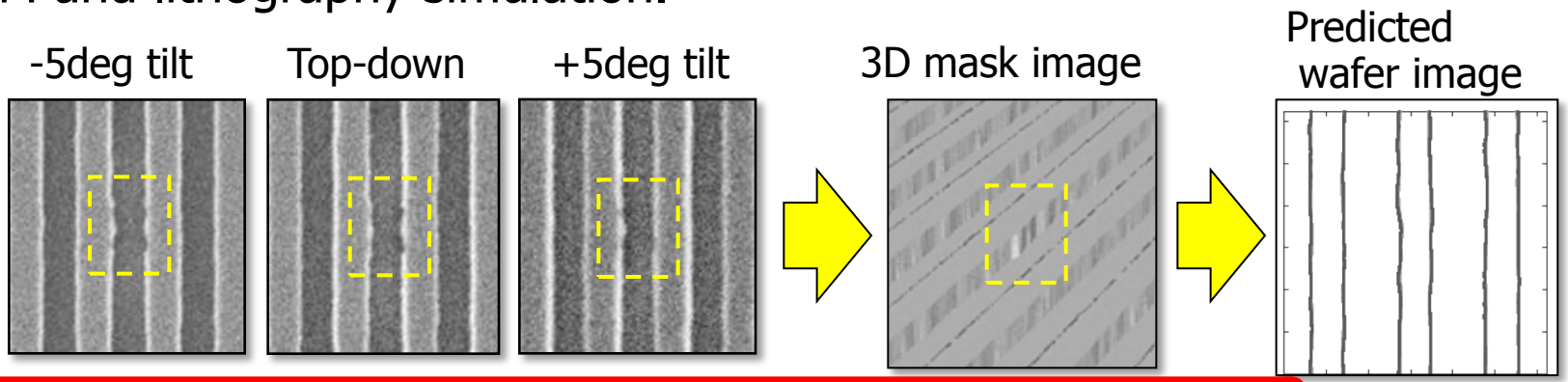


Lithography simulation

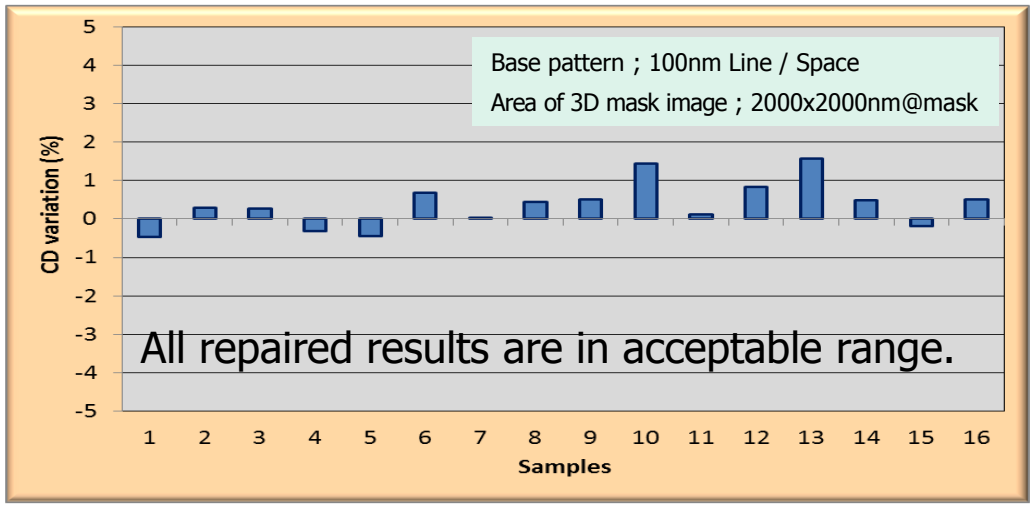
- Max. image size; 8000x8000pixels
- Max. acquisition area; 8x8um @1nm pixels
- Image distortion; <0.2%
- Tilt range; +5~-5 degrees & 4 scan rotations
- Throughput; 70min/5points

Simulated Wafer Printability Result

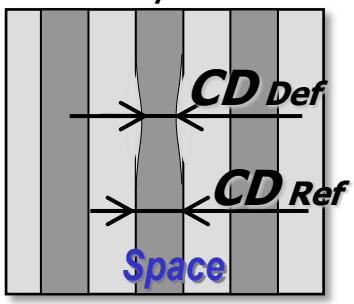
We predicted wafer printability of EB repaired absorber pattern with 3D-SEM and lithography simulation.



Repaired pattern has different side wall angle and line edge roughness.



Printability evaluation



CD variation

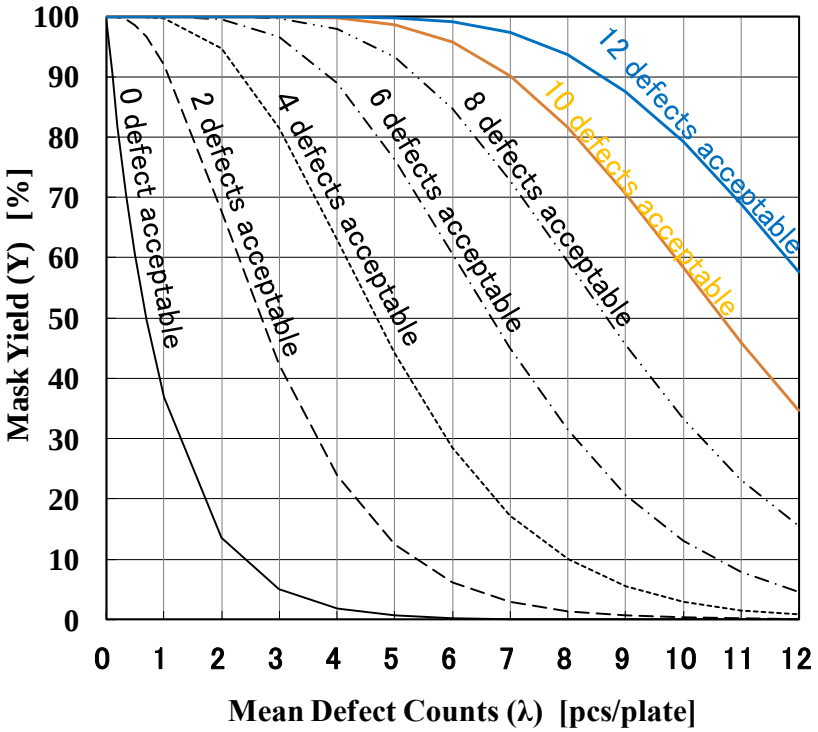
$$= \frac{CD_{Def} - CD_{Ref}}{CD_{Ref}} \times 100$$

Actual wafer printability evaluation is on-going.

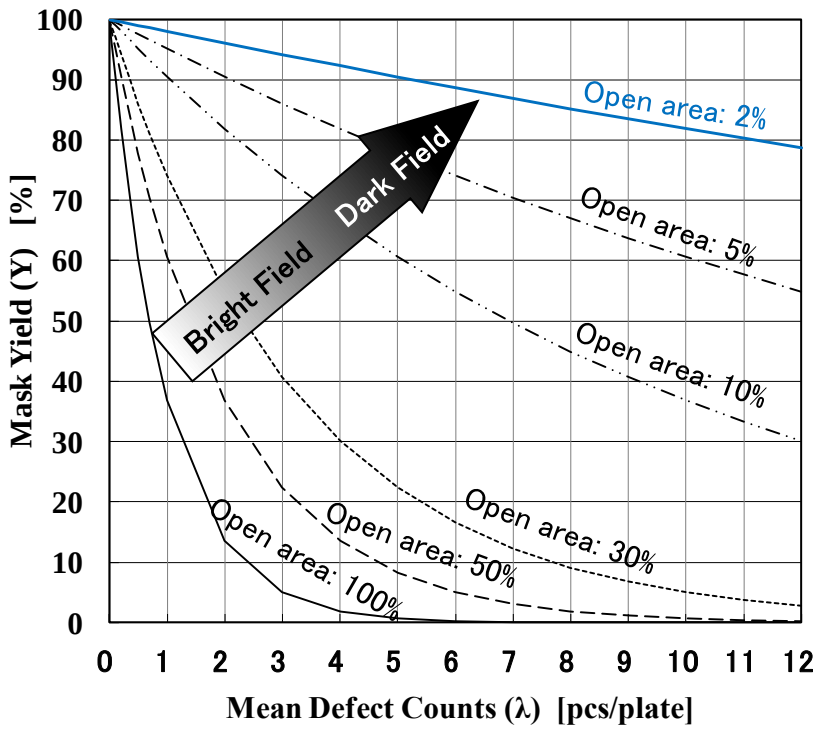
Mask Defect Yield vs Defect Counts

Estimation from Poisson Distribution

Dependency on acceptable defect counts (Bright Field)

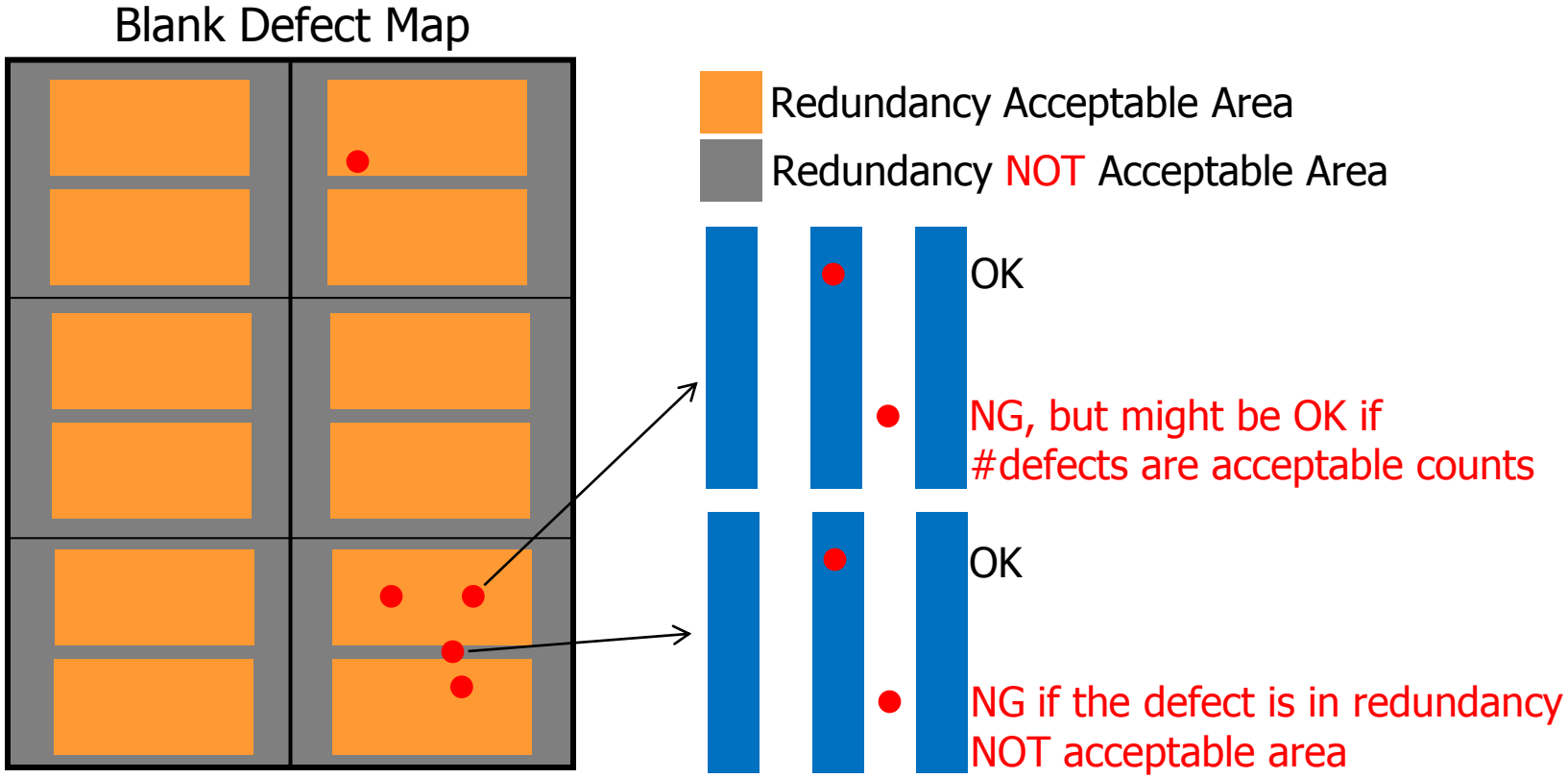


Dependency on pattern variation (Zero Defect Yield)



Blanks with small defect counts are required.

Challenges for Managing Multilayer Defect



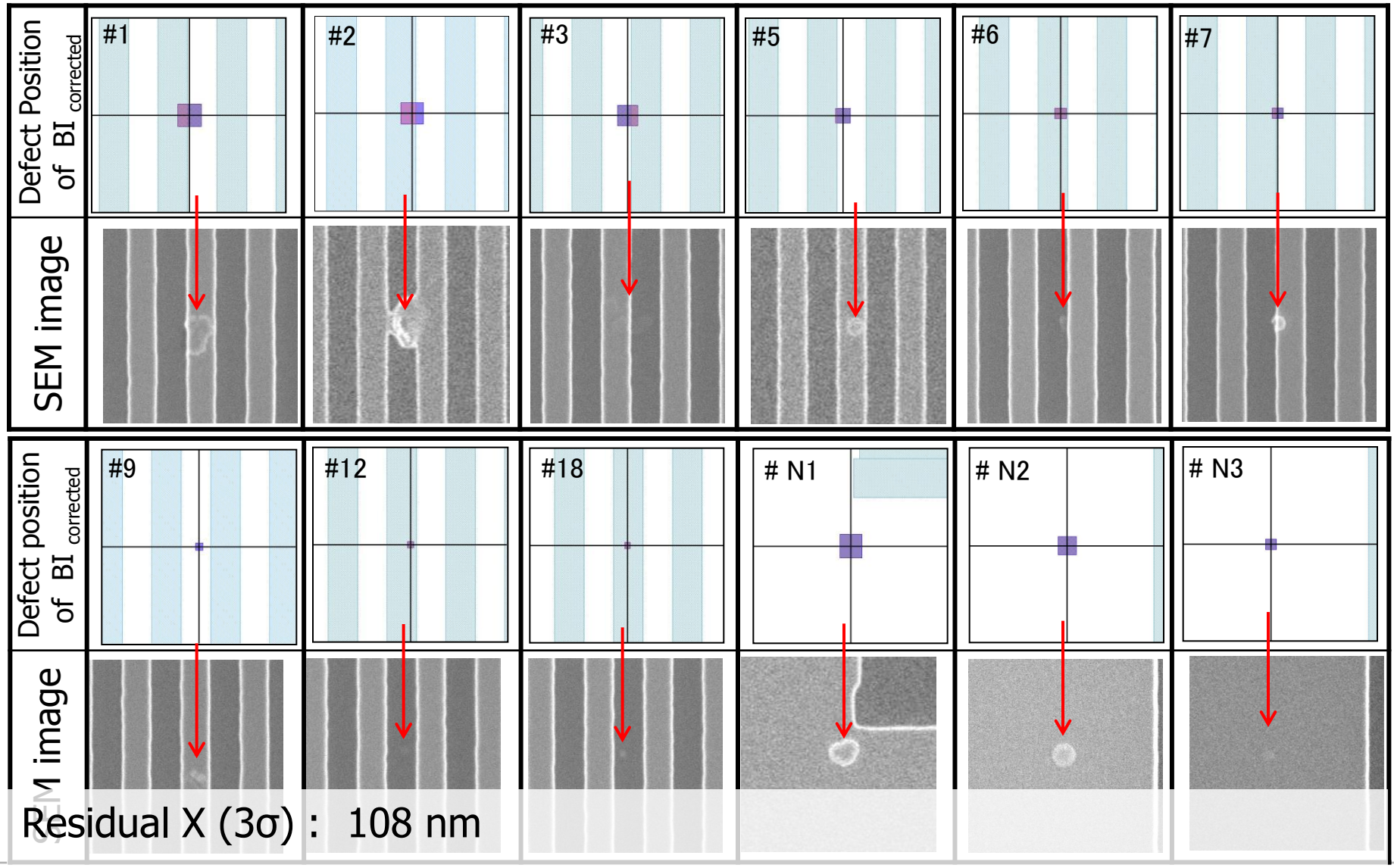
- multilayer defects :
  difficult to be identified by SEM/AFM after mask patterning

Challenges:

- Identify the position of multilayer defect (position error << pattern half pitch)
- Predict multilayer (phase) defect printability under the condition that EUV-AIMS is not available.

Defect Position Error of DUV BI Tool (3rd Gen.)

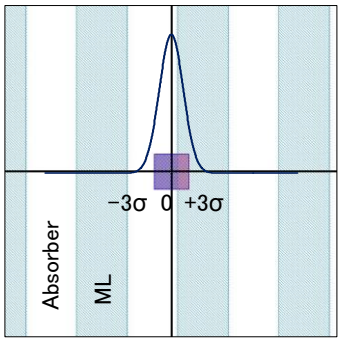
Blank defect examples identified by SEM (Mask pattern for hp3x-nm (after litho.))



Residual X (3σ) : 108 nm

Defect position error of BI coordinates is smaller than the pattern hp.

Projection Defect Size to ML

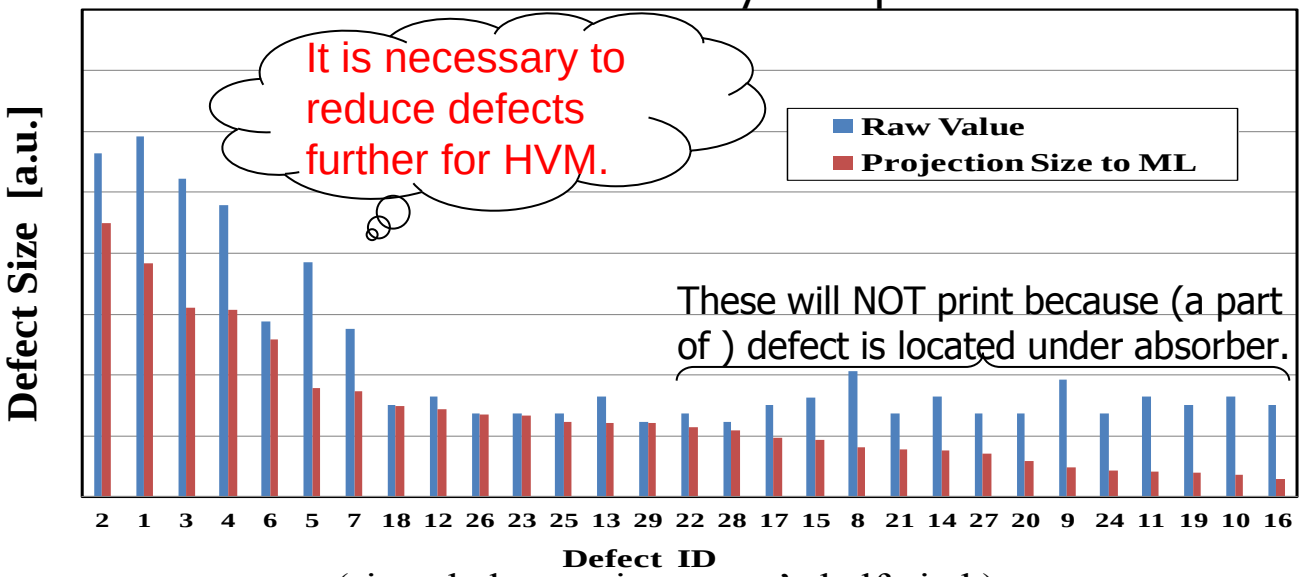


Projection Defect Size to ML (Expectation Value)

$$\int_{-3\sigma}^{+3\sigma} S(x) \cdot P(x) dx$$

S(x): projection defect size to ML
P(x): probability of defect location

Defects at Redundancy Acceptable Area

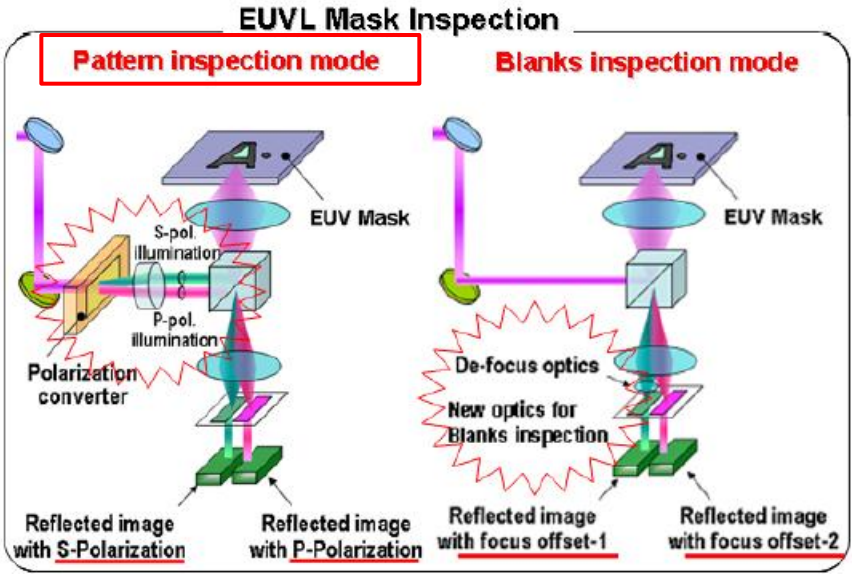


(size: below main pattern's half pitch)

The idea of projection defect size to multilayer avoids overestimating the number of potential killer defects.

Patterned Mask Inspection Tool

NPI-7000 (NuFlare)



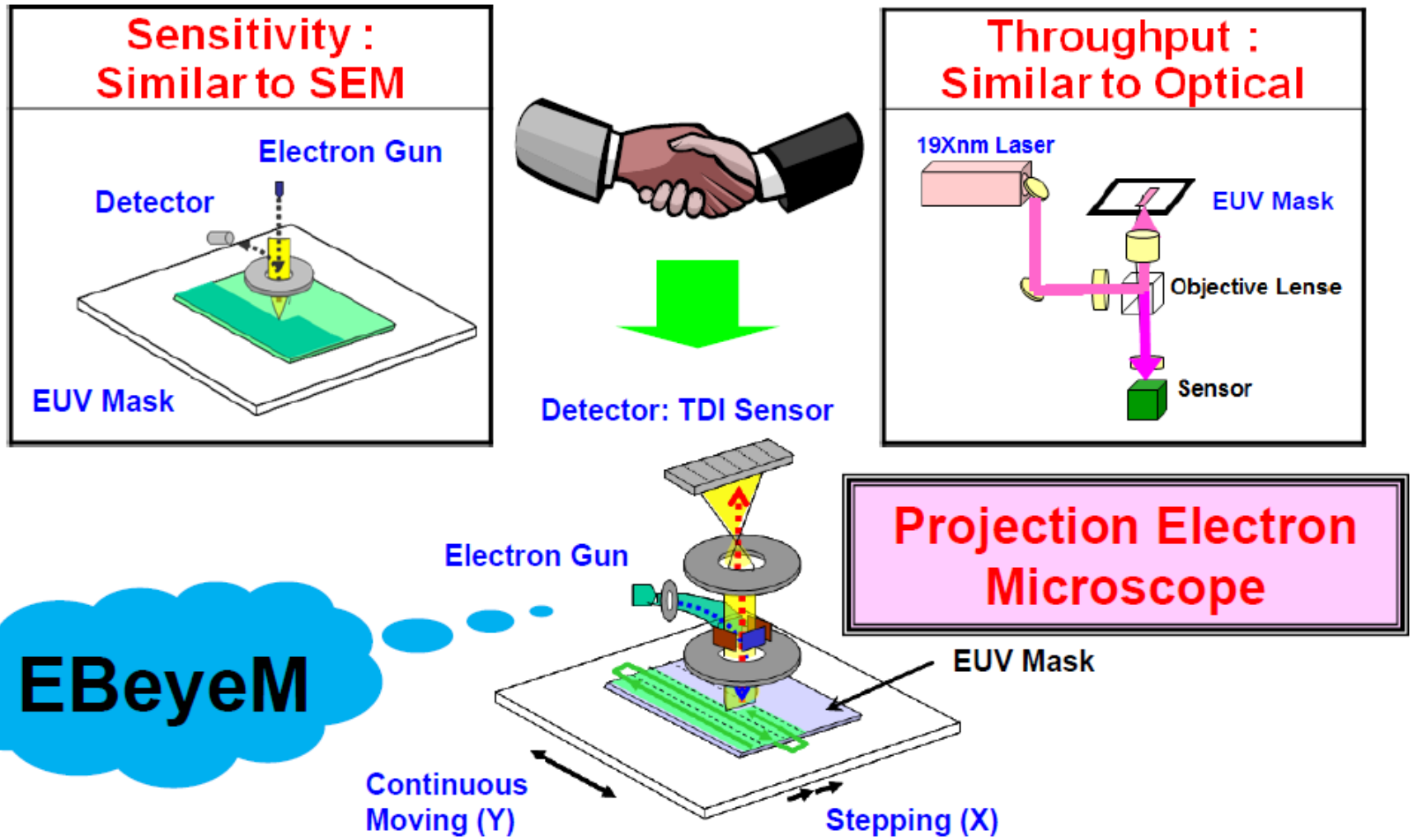
Base Pattern	Defect Type	Inspection Mode	Defect size nm (Square root of area) 80	75	70	65	60	55	50	45	40	35	30	25	20	15	10	5
32nm TN	Edge extrusiton	DD																
		D-DB																
	Edge intrusion	DD																
		D-DB																
27nm TN	Edge extrusiton	DD																
		D-DB																
	Edge intrusion	DD																
		D-DB																
22nm TN	Edge extrusiton	DD																
		D-DB																
	Edge intrusion	DD																
		D-DB																

10% CD error (Calculated)

Hirano, et al. (BACUS2010)

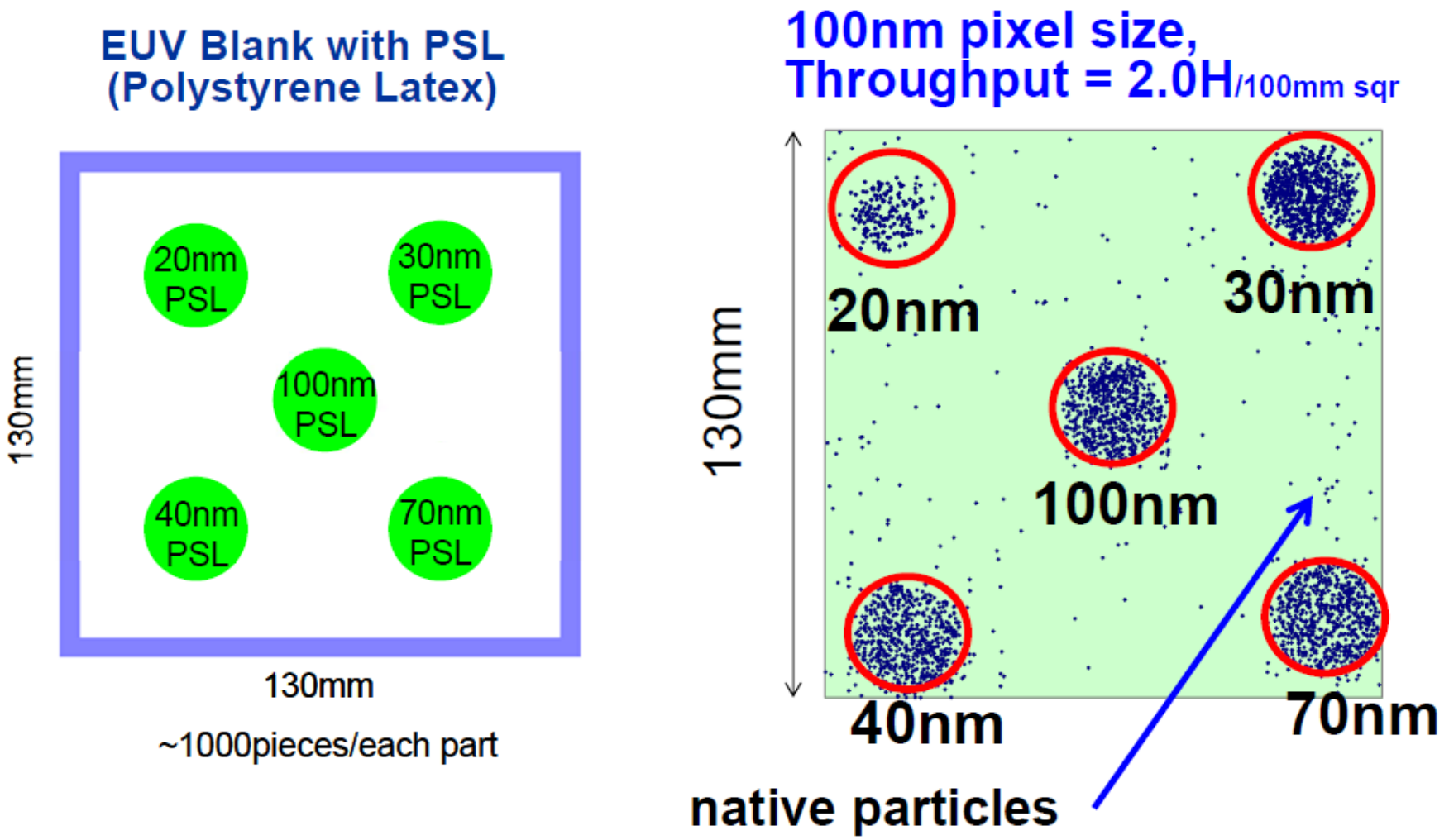
EB Inspection

EBeyeM (EBARA)



Areal illumination of PEM improves inspection throughput.

EB Inspection (Particle Inspection Mode)



EUV Mask Infrastructure Readiness

		after litho.	
		hp 3x ~ hp 2x	hp 1x
Mask QA		3D SEM + Litho. Simulation	EUV-AIMS
multilayer defect	Inspection	DUV inspection	Actinic inspection @EIDEC/Lasertec
	Mitigation	Redundancy	Redundancy
		Absorber covering (for dark field mask)	Absorber covering
			Compensation repair
absorber defect	Inspection	DUV inspection	EB inspection @EIDEC/EBARA
	Repair	EB repair	
Particle inspection		EB inspection	

ready under developing

Absorber Pattern Generation

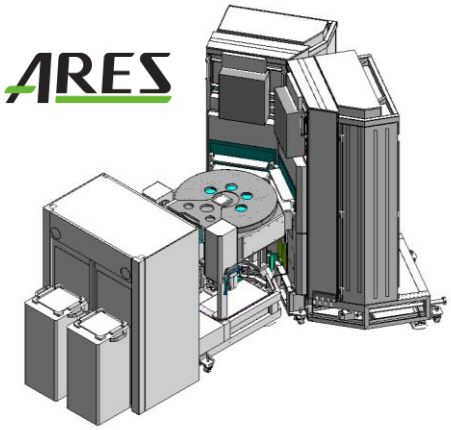
EB writer : "EBM8000"

(NuFlare)

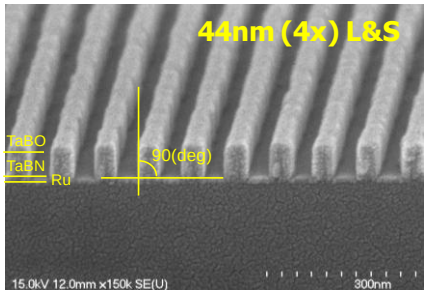
http://www.nuflare.co.jp/product/ebm.html

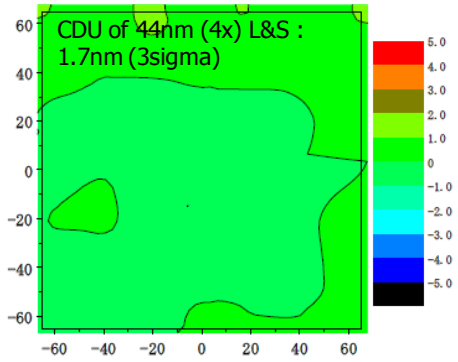
Dry Etching Equipment : "ARES$_{TM}$"

(Shibaura Mechatronics)



Iino, et al. (BACUS2010)



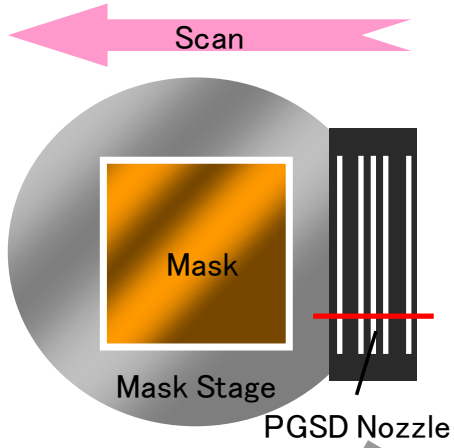


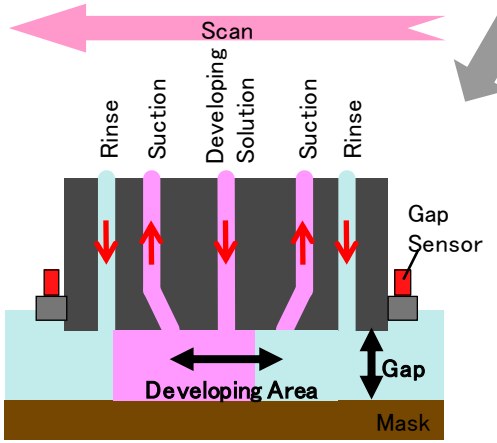
Scanning-type Developer : "PGSD"

Proximity-Gap-Suction-Development System

(Tokyo Electron)

- Slit and scan type development
- Narrow gap
- Suction slits for removing dissolution products



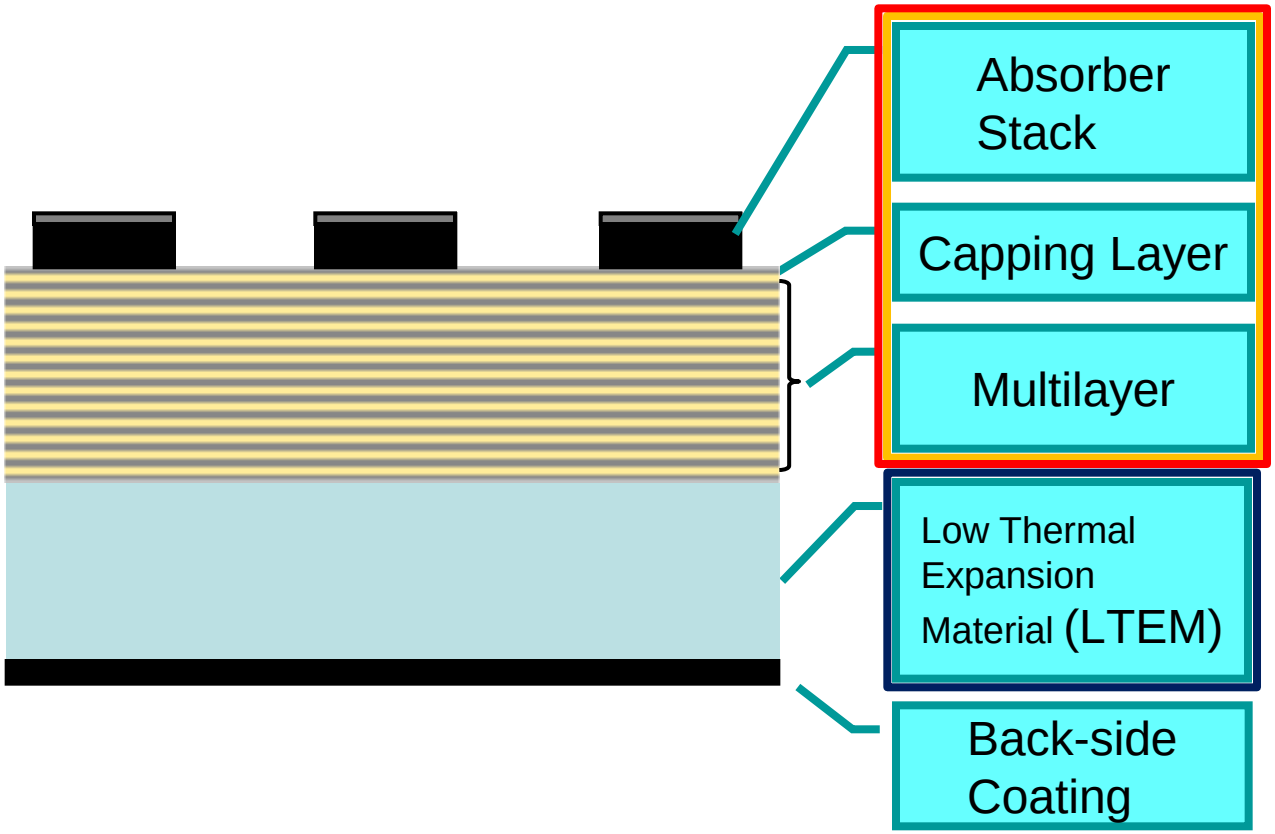


Cross-sectional view

- ✓ Extreme high uniformity of developing solution supply
- ✓ Nearly zero loading effect caused by dissolution products

Etched absorber pattern has capability for scaling down to hp1x EUVL single exposure.

EUV Mask Structure for Scaling



needs fine tuning for high throughput

needs optimization for high NA scaling

needs material change for shorter wavelength

need further R&D

Readiness and Challenges of EUV Mask

EUV masks for hp3x~2x (after litho.) /hp1x (after DP process) can be almost ready for HVM insertion.

Mask CD of absorber pattern has capability for scaling down to hp1x EUV single exposure.

Further R&D is necessary for EUV mask to scale with high NA / shorter wavelength.